IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Beshai	
Application No.: 10/054,362	
Filed: November 13, 2001	Group Art Unit: 2662
Title: DATA BURST SCHEDULING	
Attorney Docket No.: 120-212	
Nortel ref. :14880ROUS01U	Examiner: CHO, HONG SOL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 CFR 1.111

Dear Sir:

In response to the Office Action of March 15, 2006, please amend this application as shown on the attached sheets.

Amendments to the claims begin on page **2** of this paper.

Remarks/Arguments begin on page **8** of this paper.

IN THE CLAIMS:

1. (Original) A burst-switching network comprising:

a plurality of source nodes;

a plurality of upstream links coupled to said plurality of source nodes;

a plurality of sink nodes;

a plurality of downstream links coupled to said plurality of sink nodes;

a plurality of core nodes, at least one of said plurality of core nodes is coupled to a subset of said plurality of upstream links and a subset of said plurality of downstream links and has a plurality of space switches, each space switch having a slave controller; and

a plurality of master controllers in each core node, one said master controller associated with each of said plurality of space switches in each of said plurality of core nodes and a designated one of said master controllers in a core node functions as a core-node controller, said core-node controller communicatively connecting to each of said master controllers,

said core-node controller operable to:

receive control data from at least one of said plurality of source nodes;

divide said control data among said master controllers; and

instruct each master controller to generate a burst-switching schedule for a space switch associated with said each master controller, communicate said schedule to a respective edge node, and transmit instructions based on said schedule to a slave controller of said space switch after a pre-calculated delay period.

2. (Original) The network of claim 1 wherein each of said plurality of source nodes is paired with a corresponding one of said plurality of sink nodes to form a plurality of network edge nodes.

3. (Original) The network of claim 2 wherein at least one of said plurality of space switches is an optical switch.

4. (Original) The network of claim 3 wherein any of said master controllers can be designated to function as a core-node controller.

5. (Original) The network of claim 4 wherein said pre-calculated delay period exceeds the round-trip delay between said core node and said respective edge node.

6. (Original) The network of claim 4 wherein each of said master controllers includes a burst scheduler.

7. (Original) The network of claim 6 wherein said burst scheduler computes a burst-transfer schedule for a plurality of space switches.

8. (Original) The network of claim 7 wherein each of said space switches has a plurality of burst-mode input ports, from each of which individual data bursts are directed to output ports of the space switch, and a plurality of channel-mode input ports, the entire data from each of which is directed to a respective output port of the space switch.

9. (Original) The burst-switching network of claim 1 wherein each of said plurality of master controllers comprises:

an input interface for receiving upstream control bursts from a source node;

an input interface to receive control data from a core-node controller;

a burst scheduler for generating a schedule for operation of at least one space switch;

an output interface for communicating said schedule to a sink node associated with said source node;

a transmitter operative to transmit instructions to a slave controller of each of said at least one space switch, where said instructions are based on said schedule; and

a device to acquire timing data from an upstream control burst.

10. (Currently Amended) In a bufferless space switch having a plurality of burst-mode input ports and a plurality of output ports, a method of determining a schedule for switching

data bursts, over a designated schedule period T, from said plurality of burst-mode input ports to said plurality of output ports, the method including the steps of:

generating said schedule for a succession of bursts occupying said designated schedule period T, said generating being implemented every time period of a multiple m of said designated schedule period T; and

repetitively employing said schedule for switching data bursts during m consecutive periods, m being an integer greater than zero and each of said consecutive periods is equal to said designated schedule period T;

wherein m is selected to exceed a ratio of a computation time of said schedule and said designated schedule period T.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Currently amended) The method of claim ~~13~~ 10 including the further step of generating said succession of bursts according to bitrate allocations for burst streams to be switched from a burst-mode input port to an output port.

15. (Original) The method of claim 14 including the further step of refreshing said bitrate allocations periodically every m × T interval.

16. (Currently amended) In a bufferless space switch having a plurality of burst-mode input ports and a plurality of output ports, a method of determining a schedule for switching data bursts, over each of successive time intervals, each time interval having a duration T, from said plurality of burst-mode input ports to said plurality of output ports, comprising the steps of:

setting ~~the~~ a computation period for each of said successive time intervals to an integer multiple m of the interval T; and

concurrently computing m successive schedules; ~~concurrently~~

wherein m is selected to exceed a ratio of a computation time of said schedule for said each of successive time intervals and said duration T.

17. (Cancelled)

18. (Cancelled)

19. (Currently amended) The method of claim ~~18~~ 16 including the further steps of computing said schedule for burst descriptors generated according to bitrate allocations for each pair of burst-mode input port and output port, and refreshing the bitrate allocations at every interval T.

20. (Original) A method of computing a burst-switching schedule in a bufferless space switch having a plurality of burst-mode input ports, the method comprising steps of :

a. receiving burst descriptors associated with each of the plurality of burst-mode input ports;

b. placing said burst descriptors in bursts queues, at least one queue being associated with each one of said plurality of burst-mode input ports;

c. cyclically accessing said burst queues, determining corresponding input free time and selecting a maximum of Q candidate burst descriptors;

d. determining free time for output port indicated in each candidate burst descriptor;

e. determining the absolute value W of the difference between the output-free time corresponding to each of the Q burst descriptors and said input free time; and

f. selecting the candidate burst yielding the least value W.

21. (Original) The method of claim 20 including the further step of determining said burst descriptors at edge nodes in a closed-loop burst-transfer-control system.

22. (Original) The method of claim 20 including the further step of determining said burst descriptors at core nodes in a closed-loop burst-transfer-control system.

23. (Original) The method of claim 22 where each of said burst descriptors is associated with a burst stream and said determining is based on a bitrate allocation for said burst stream.

24. (Original) A burst scheduler for a space switch, said space switch having a plurality of input ports and a plurality of output ports, said scheduler including:

a receiver for receiving burst descriptors and placing each of said burst descriptors in one of a plurality burst-descriptor memories, each of said burst descriptors identifying an input port, an output port, and a burst size;

an input-state memory for storing next available time of each of said input ports;

a plurality of output-state memories, each storing next-available time of each of said output ports;

a processing circuit including a scheduler kernel for computing a schedule for burst-transfer across said space switch over a predefined period of time T, said processing circuit operable to

select a number Q of candidate burst descriptors for each input port, where Q is an integer greater than zero;

compare corresponding entries in said input-state memory and said plurality of output-state memories for each of said Q candidate burst descriptors and determine a corresponding merit index; and

select one of said Q candidate burst descriptors according to said merit index;

and

a permits buffer for storing said schedule.

25. (Original) The burst scheduler of claim 24 wherein said merit index is based on an absolute value of the difference between said corresponding entries.

26. (Original) The burst scheduler of claim 24 wherein each of said burst-descriptor memories is operative to store burst descriptors belonging to a subset of burst-switching input ports.

27. (Original) The burst scheduler of claim 24 wherein the output-state memories have identical content.

28. (Original) The burst scheduler of claim 24 wherein the output-state memories are read concurrently at arbitrary memory addresses.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Original) In a core node having a plurality of space switches operated in parallel, each of said plurality of space switches having a plurality of input ports, a plurality of output ports, and a master controller with one said master controller designated to function as a core-node controller, said core node switching burst streams from a plurality of upstream links, each having multiple wavelength channels, to a plurality of downstream links, each having multiple wavelength channels, a method of confining connections from each upstream link to each downstream link to a small number of space switches, the method comprising the steps of:

receiving a bitrate requirement for each connection;

sorting received bitrate requirements associated with each upstream link in a descending order according to bitrate value;

implementing a cyclic allocation of said requirements to corresponding paths of the space switches, retaining a remainder when one of said corresponding paths is exhausted, and determining a progress indicator; and

repeating said cyclic allocation if permitted by said progress indicator.

REMARKS

Claims 11-13 and 17-18 are cancelled by way of this amendment. Claims 1-10, 14-16, 19-28 and 32 are currently pending. Claims 29-31 were previously cancelled. Reconsideration and further examination is respectfully requested.

Claim Objections

Claim 10 is objected to because of informality. The claim has been amended as suggested by the Examiner.

Rejections under 35 U.S.C. §102 and 103

Claims 10-19 were rejected under 35 U.S.C. §102(e) as being anticipated by Xiong et al. (US Pub. 2002/0118421).

The Xiong Reference

Xiong discloses an optical burst switched network which includes multiple electronic ingress edge routers and multiple egress edge routers. The ingress edge routers and egress edge routers are coupled to multiple core optical routers. The basic data block to be transferred is a burst which consists of a burst payload (called "data burst") and a burst header. A data burst and its header are transmitted on different channels and the header is sent ahead of its associated data burst with an offset time. A discrete-time network-control system is used, with the basic time unit, called a time-slot, being used for organizing data transmission. Control data transmitted over a control channel may be organized in data blocks each of a duration called 'timeframe' that may include several time units (several time slots).

In the network of Xiong, an edge router sends a burst header to an optical core router then follows the header with the burst data without waiting for acceptance. The burst data may be discarded by the optical core node if it cannot be accommodated.

Each optical core router comprises an optical-switch-matrix which is configured periodically, i.e., the input-output internal paths within the optical-switch-matrix may change every "configuration period". The configuration period could be a single time slot or a

multiple of time slots. Data bursts may be of variable length; however, each data burst is considered to occupy an integer number of time slots.

FIGS. 4a and 4b in Xiong clearly illustrate the timing system. Each of FIG. 4a and FIG. 4b illustrates a data burst (denoted DB) occupying seven time slots (time slots 15 to 21), with the timeframe of the control channel set equal to one time slot in FIG. 4a and four time slots in FIG. 4b. The burst header (denoted "burst-header packet" BHP) of the data burst is sent earlier (ahead of the data burst) over a separate control channel.

In the network of Xiong, an optical core node handles data bursts individually as they arrive and hence, **it cannot possibly generate a schedule and use the schedule periodically** as stipulated in claim 10 of the present invention.

Applicant's Specification

In the burst-switched network described in Applicant's specification, rather than sending bursts preceded by their headers to an optical core node, each edge router (source node) determines its bitrate requirements for paths to each other edge router (sink node) and sends **bitrate-allocation requests** to a selected core-node controller which computes permissible burst sizes and corresponding burst-transfer schedules over a pre-defined time interval called a "schedule period". The schedule period may accommodate a large number of data bursts. The controller of the selected optical core node sends details of the permissible burst sizes and corresponding burst-transfer instants of time to corresponding edge routers. The network of the present invention employs a novel technique of "time-locking" which enables each edge node to send bursts to arrive at the selected core node at the specified time instants despite the propagation delay which varies according to the transmission distance and may also vary slowly with time due to some factors. This scheme significantly simplifies the network operation and **prevents data loss** at the optical core node (a burst cannot be discarded).

In a large-scale optical core node, having a large number of input ports and output ports, computing a schedule for permissible bursts over a 'schedule period' may require a computation time that exceeds the schedule period. To circumvent this problem, two schemes are provided. The first scheme, described in claim 10 and illustrated in FIG. 26 of the present application uses a single processor and refreshes the generated schedule every time interval that may cover several schedule periods (four for example, as illustrated in FIG. 26). The

second scheme uses multiple processors which, collectively, generate a new schedule every schedule time as illustrated in FIG. 27 of the present application which uses four processors.

Claim Rejections – USC 102

In order to support a rejection under 35 U.S.C. §102, every limitation in the claims must be shown or suggested by the reference. Applicant respectfully submits that Xiang fails to show or describe several limitations in the claims.

For example, Applicant's claim 10 recites "... a method of determining a schedule for switching data bursts, over a designated schedule period T, ...the method including the steps of ... generating said schedule for *a succession of bursts occupying said designated schedule period T*, said generating being implemented every time period of a multiple m of said designated schedule period T; and repetitively employing said schedule for switching data bursts during m consecutive periods, m being an integer greater than zero and each of said consecutive periods is equal to said designated schedule period T ... wherein m is selected to exceed a ratio of a computation time of said schedule and said designated schedule period T...."

In rejecting claim 10, the Examiner appears to equate the process in Xiong of configuring the optical switch matrix periodically over one time slot period with the process of determining a schedule for switching data bursts over a designated schedule period. The Examiner referenced paragraph [0069] in Xiong. Applicant respectfully notes **that a burst in Xiong occupies several time slots while a schedule period in the present invention includes "a succession" of bursts. There is no resemblance whatsoever between a time slot in Xiong and a schedule period as defined in the present application.**

The Examiner further equates 'using a time slot for switching data bursts' in Xiong with 'repetitively employing a schedule for switching data bursts during m consecutive periods ….". Reference is made to paragraph [0069], lines 7-9 of Xiong. Applicant respectfully notes that lines 7-9 in paragraph [0069] refer to the use of a time slot as a basic time unit. As illustrated in FIGS. 4A and 4B in Xiong, a data burst (marked 'DB') has a length of seven time slots.

Please see page 23, lines 8-12, and page 39, lines 11-12, of the present application:

"The **schedule period must exceed the duration of the longest burst received at a core node**. In order to simplify time coordination between a core node and an edge node, it is preferable that a time-counter cycle period (master cycle period) be an integer multiple J of the schedule period. Furthermore, it is preferable that the integer multiple J be a power of two."

"The bursts generated by a burst-stream generator 2120 are grouped into burst sets, where **each burst set occupies a schedule period** 1230 (FIG. 12)."

To improve clarity, Applicant amended claim 10 to include the limitations of claim 11, 12, and 13. Claims 11, 12, and 13 are therefore cancelled. For at least the reason that Xiong fails to describe or suggest the step of 'generating a schedule of a succession of bursts occupying the designated schedule period T", it is respectfully requested that the rejection under 35 U.S.C. §102 be withdrawn.

Regarding claim 14, claim 14 depends upon claim 10 and is patentable for at least the same reasons as claim 10. However, claim 14 also includes several elements that distinguish the claim from the system of Xiong. For example, although the Examiner asserts that Xiong discloses inherently generating continuous bursts periodically in time slots with a given number of bits, Applicant respectfully notes that **Xiong does not generate bursts, as recited in claim 14 of the present application**. Burst headers and corresponding data bursts are sent from edge routers to optical core routers and are not periodic except, perhaps, by mere coincidence. Furthermore, the novel concept of using bit-rate allocations as the basis for generating burst specification is not disclosed in Xiong. Applicant could not find any suggestion, explicit or implicit, of using bit rates for data streams as the basis for burst generation and scheduling in Xiong. This is understandable because Xiong uses the conventional burst-transfer method known as "just-in-time" (please see paragraph [0060] in Xiong which does not employ any form of flow-rate regulation. Accordingly, claim 14 is patentably distinct over Xiong for this additional reason and it is respectfully requested that the rejection be withdrawn.

Regarding claim 15, the Examiner asserts that Xiong discloses synchronizing bitrate allocations periodically in every time slot for slotted transmission. Applicant respectfully notes that Xiong does not use the concept of bitrate allocations as recited in claim 15.

Rather, lines 13-15 of paragraph [0068] in Xiong refer to the inclusion of overhead bits for the purpose of synchronization. Claim 15 of the present application discloses a step of modifying the bitrate allocations for burst streams in order to follow temporal traffic variations. The bitrate allocations are completely independent of any synchronization process. For at least the reason that no such structure is shown or suggested by Xiong, it is respectfully requested that the rejection be withdrawn.

Independent claim 16 recites "... In a bufferless space switch ... a method of determining a schedule for switching data bursts, over each of successive time intervals, ... from said plurality of burst-mode input ports to said plurality of output ports, comprising the steps of ... setting a computation period for each of said successive time intervals to an integer multiple m of the interval T; and *concurrently computing m successive schedules wherein m is selected to exceed a ratio of a computation time of said schedule for said each of successive time intervals and said duration T...*" Thus claim 16 includes limitation similar to those of claim 10, and therefore the arguments set forth with respect to claim 10 apply. The Examiner further asserts that Xiong discloses parallel scheduling of data bursts, reference is made to paragraph [0069] lines 1, 4, and 5. Applicant respectfully notes that the referenced passage refers to reconfiguring the optical switch matrix every period of multiple time slots instead of every time slot and does not suggest or imply parallel scheduling. Accordingly, for at least the reason that Xiong fails to describe or suggest every element of the claim, the rejection is overcome and should be withdrawn.

Claims 17 and 18 have been cancelled by way of this amendment without prejudice or disclaimer regarding the content therein.

Regarding claim 19, the Examiner asserts that Xiong discloses computing a schedule for burst descriptors generated according to bitrate allocations for each pair of burst-mode input port and output port. Applicant respectfully notes that the novel concept of generating burst descriptors based on bitrate allocations is not mentioned or implied anywhere in Xiong. The referenced paragraph [0064] describes the use of multiple virtual queues to handle different service classes.

Allowed Subject Matter

Applicant thanks the Examiner for the indication that claims 1-9, 20-28 and 32 are allowed. Applicant has made a diligent effort to place the application in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Lindsay G. McGuinness, Applicant's Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

In view of the above amendments and arguments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

__6/15/2006_____ __/Lindsay G. McGuinness/_____

Date

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Docket No. 14880ROUS01U/ 120-212

Dd: 6/15/2006